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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,813	12/21/2000	Marwan A. Orfali	RA-5339	2599

7590

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EXAMINER

BONZO, BRYCE P

ART UNIT	PAPER NUMBER
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2184

DATE MAILED: 08/13/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

82

Office Action Summary

Application No.

09/745,813

Applicant(s)

ORFALI, MARWAN A.

Examiner

Bryce P Bonzo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-12 and 14-19 is/are rejected.
- 7) ☒ Claim(s) 6, 13, 20 and 21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 April 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1, 9-12, 14 and 16-19 are rejected under 35 USC §102.

5 Claims 2-5, 7 and 15 are rejected under 35 USC §103.

Claims 2, 8 and 15 are rejected under 35 USC §112.

Claim 1 is objected to based on one minor informality.

Claims 6, 13, 20 and 21 are indicated as containing allowable matter.

10 ***Objections to the Specification and Drawings***

For clarity Applicant is requested to renumber the drawings and description of the drawings to be consecutive. The lack of a Figure 11 and its recitation in the Brief Description of the Drawings as not existing, causes confusion.

Applicant is required to provide the cross referenced Application Numbers
15 omitted on page 1.

Page 27, lines 18-20 recite "pooling." It is believed Applicant intends to use the term "spooling."

The Examiner objects to applicant's use of the term "spooling." As further described below in the rejection of claims 2 and 15, "spooling" is a process which
20 requires the data transferred to be acted on while the transfer is in progress, inherently contradicted by Applicant's specification and claims, which describe the acting upon the data at some later point.

Rejections under 35 USC §112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

5 The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 8 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10 Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed.
15 Cir. 1999). The term “later spooling” in claims 2 and 15 is used by the claim to mean “memory can be offloaded into permanent storage systems attached to the PC-type collector computer system for analysis at leisure after the trace is completed”(page 6 of the specification), while the accepted meaning is “To read input, or write output data, to auxiliary or main storage for later processing or output, in order to permit input/output
20 devices to operate concurrently with job execution.” The term is indefinite because the specification does not clearly redefine the term. Applicant has described the well known process of “flushing” memory temporary to permanent memory. Both “flushing” and “spooling” have distinct meanings as provided in the attached IEEE and Microsoft Dictionary passages. Further page 27, lines 18-20 describe a process “pooling” that is

in fact "flushing". Particular evidence that "spooling" is not occurring is that the data transferred to the permanent storage for detailed analysis at the user's leisure. A system which incorporates "spooling" will begin to immediately process data, as soon as enough data has arrived to begin processing. This practice was widely used in printers
5 prior to the availability of inexpensive RAM and high speed USB and Ethernet connections. Prior to these innovations, printers did have the required RAM to store an entire document and the communication channel used to transfer data to the printer was enough that initiating printing prior to receipt of an entire document significantly decreased overall print time.

10 As per claims 8, Applicant recites "an interposer interposed between a processor.." and does not finish the claim by stating what else the interposer is between. Applicant is required to amend the claim to create a complete and consistent thought.

15 ***Objections to the Claims***

Claim 1, line 19 recites "said bus processor speed" without previously reciting a bus. It is believed Applicant intended to recite "said processor interconnect speed." As bus and processor are synonyms for each other in the computer arts, the Examiner is able to discern the scope of the claim. Applicant is requested to however, modify the
20 claim to ensure strict antecedent basis.

In claim 1, line 9 the Examiner believes that "of" should be placed between *identification* and *all*.

In claim 3, line 2 "said" is inadvertently repeated. Applicant is requested to correct this issue.

Rejections under 35 USC §102

5 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

10 (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 ,4, 5, 7, 9-12, 14 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by La Jolie et al (United States Patent No. 5,933,594).

15 As per claim 1, La Jolie discloses:

an input channel circuit for receiving all activity on a high speed interconnect in a system under test (column 3, lines 43-56, in particular 44-46),

a preview pipeline circuit connected to monitor said input channel for capturing all occurrences of said high-speed processor interconnect signals at processor speed
20 (column 3, lines 43-56; column 3, lines 34-48),

a trigger circuit maintaining a predetermined trigger value to compare against said all occurrences (column 13, lines 36-48), and to trigger identification all of said high-speed processor interconnect signals associated with each appearance of a trigger signal equivalent to said predetermined trigger value in said occurrences captured by
25 said pipeline circuit (column 14, lines 1-34) and to pass each instance of said

occurrences which are associated with a said appearance of a trigger signal as a word to a compaction circuit (column 15, lines 23-34),

a time stamp generating circuit for generating a time stamp value signal for each said occurrence and associating a one of said time stamp values associated with one of

5 said each occurrences (column 14, lines 19-25),

said compaction circuit for eliminating any wasted space within said word and passing compacted sets of such words as an entry signal on to a high speed FIFO memory at said bus processor speed (column 16, lines 2-19; column 16, lines 27-38), each of said words in said compacted set of words being passed with an associated

10 time stamp value signal (column 16, lines 48-62),

said high speed FIFO memory operating at said high-speed processor interconnect speed for receiving said entry signals at said high-speed processor interconnect speed (column 18, lines 48-60) for providing that each of said entry signals is associated with a said associated one of said time stamp value signals (column 16, lines 48-51), and for providing a said entry and its said associated time stamp value signals to an output channel (column 12, lines 40-47).

As per claims 9, La Joie discloses:

wherein said FIFO memory has sufficient capacity for holding at least two kilo-
20 entry signals (column 11, lines 21-33; the memory is access in 4 kilo-entry DMAs and therefore must have at least 2 kilo-entries of data in the FIFO).

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As per claim 10, La Joie discloses:

where in said FIFO has sufficient capacity for handling between two kilo-entry and 16 kilo-entry signals (column 11, lines 21-33; the memory is access in 4 kilo-entry DMAs and therefore must have at least 4 kilo-entries of data in the FIFO, falling inside

5 Applicant's claimed range).

As per claim 11, La Joie discloses:

wherein said FIFO memory has sufficient capacity to handle anticipated burstiness of software in use on a system under test (column 18, lines 48-50; column
10 11, lines 21-32; column 10, lines 9-60; La Joie clearly has considered burstiness and describes it as a factor in designing the system, further the 4K DMAs out of the FIFO ensure the FIFO never overflows and is therefore always large enough for burstiness).

As per claim 12, La Joie discloses:

15 wherein said compaction circuit comprises control logic settable to determine specific bytes of a word to be selected down to (column 15, lines 26-33).

As per claim 14, La Joie discloses:

a. connecting to a high speed interconnect from which to receive processor
20 signals on an input channel (column 3, lines 43-56),

b. receiving signals from said high speed interconnect at a clock speed matching said high speed interconnect in a collector computer system (column 9, lines 53-54),

c. setting up said collector computer system to receive said signals upon initiation of said collector computer system (column 8, line 64 to column 11, line 20 specifically describe many such issues to consider when setting up this type of system), whereupon said collector computer system monitors said input channel for said received signals
5 and captures said received signals as input words (column 3, lines 57-67),

d. generating a time stamp value for each input word, and associating each generated time stamp value with said input word signal (column 14, lines 19-25),

e. monitoring said input words for an appearance of a trigger signal (column 16, lines 2-19; column 16, lines 27-28), and

10 f. storing only entry word signals associated with each said appearance of a trigger signal during a tracing period into a high speed FIFO memory together with its associated time stamp value as entry signals (column 18, lines 48-60; column 12, lines 40-47).

15 As per claim 16, La Joie discloses:

wherein in said connecting step (a) said connection to said high speed interconnect is made to a high speed processor bus (column 5, lines 43-44; column 3,, lines 57-60) and said processor signals are in a bus protocol format and wherein an additional step aligns each series of a bus protocol word series into a single word of
20 said entry words (column 7, lines 34-40; column 9, lines 39 through column 10, line 8).

As per claim 17, La Joie discloses:

wherein said entry word associated with each said trigger signal comprise a predetermined number of entry word signals immediately preceding an occurrence of a trigger plus a predetermined number of said entry word signals immediately following

5 said occurrence of said a trigger signal (column 14, lines 16-19).

As per claim 18, La Joie discloses:

wherein at least one of said predetermined numbers of entry words is a zero (column 16, lines 14-19; zero is the minimum value for a physical storage and La Joie

10 describes it may be desirous to operate at the minimum in some cases).

As per claim 19, La Joie discloses:

wherein said step (f) further comprises compacting said entry words associated with a said trigger signal prior to said storing (column 15, lines 47 through column 16,

15 line 7).

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over La Joie et al (United States Patent No. 5,933,594) .

As per claim 2, La Joie discloses:

The apparatus of claim 1 (as described in the rejection of claim 1); a collector computer system having a channel to receive said entry signals from said output channel (column 12, lines 26-47) and to store them in main memory (column 7, lines 48-65) . La Joie further discloses the transferring of the data to permanent memory storage (column 7, lines 48- column 8, lines 10).

La joie does not explicitly disclose the later spooling of data in main memory to permanent memory. As described above in the rejections under 35 USC §112, "spooling" is used repugnant to its accepted meaning, and based on the specification this claims are interpreted as referring the process of flushing memory from main to permanent memory. The concept of flushing is shown in the IEEE Dictionary and Microsoft Dictionary, as a well known process by which main memory is transferred to permanent storage. Then the main memory is available for further use. This process is

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often used in virtual memory, FTP, updating and virtual memory systems. It allows the computer to store the data as it arrives and then efficiently transfer it to permanent storage. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the to carry out memory flushing, in order to carry out memory transfer operations creating a system which offers the debugging facilities of La Joie while operating in the a conventional manner within the collector's memory system.

As per claim 15, La Joie discloses:

The method of claim 14 (as described in the rejection of claim 14).

La Joie does further discloses the passing entries from said FIFO to a collector system main memory (column 11, lines 21-33). La Joie further discloses the transfer to permanent storage (column 7, lines 48- column 8, lines 10). La Joie does not explicitly disclose the later spooling of data in main memory to permanent memory. As described above in the rejections under 35 USC §112, "spooling" is used repugnant to its accepted meaning, and based on the specification this claims are interpreted as referring the process of flushing memory from main to permanent memory. The concept of flushing is shown in the IEEE Dictionary and Microsoft Dictionary, as a well known process by which main memory is transferred to permanent storage. Then the main memory is available for further use. This process is often used in virtual memory, FTP, updating and virtual memory systems. It allows the computer to store the data as it arrives and then efficiently transfer it to permanent storage. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the to

carry out memory flushing, in order to carry out memory transfer operations creating a system which offers the debugging facilities of La Joie while operating in the a conventional manner within the collector's memory system.

5 Claims 3-5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over La Joie et al (United States Patent No. 5,933,594) in view of Beck et al. (United States Patent No. 6,396,517 B1).

As per claim 3, La Joie discloses:

10 Apparatus as set forth in claim 2 (as set forth in the single reference 35 USC §103 rejection above). La Joie does not explicitly disclose wherein a console is associated with said collector computer system and wherein said console provides a user interface by which said trigger can be set to at least one trigger value as desired by a user at said console. These features are described in Beck at column 6, lines 19-38
15 and Figure 1. The description of an operator selecting the relative positioning and interrelationships of the selected trigger functions clearly describes a console environment on a computer used in trace collection and the modifying of the trigger conditions. Beck states the difficulty of designing triggering systems for bus event tracing and a long history of the problems of doing bus event tracing without a simplified
20 user console used to define triggers (Beck: column 2, lines 25-36). La Joie further discloses embodiments which make use of resources beyond the trace analyzer directly coupled to the system under test, such as external storage for large amounts of data

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(La Joie: column 7, lines 6 through column 8, line 10). La Joie further describes other instances where it is advantageous to control the logic analyzer completely from a remote computer (La Joie: column 12, lines 26-8). Thus it would have been obvious to one of ordinary skill in the art at the time of invention to provide the console and trigger definition system of Beck into the trace analyzer of La Joie which has been already adapted to interface with external support systems in order to create a trace analyzer with an easier to use trace configuration console, and therefore creating an easier to use system which is less prone to error and hardship in the trigger definition phase prior to running a trace analysis.

10

As per claim 4, La Joie discloses:

wherein said trigger set to at least one trigger value as desired includes trigger corresponding to address range values in said system under test (La Joie: column 5, lines 45-47).

15

As per claim 5, La Joie discloses:

wherein said trigger set to at least one trigger value as desired includes trigger value corresponding to address/function values in said system under test (La Joie: column 5, lines 45-47).

20

As per claim 7, La Joie discloses:

wherein said trigger set to at least one trigger value as desired includes pulse occurrences on identified lines of said input channel (La Joie: column 6, lines 56-61).

5

Allowable Matter

Claims 6, 13, 20 and 21 contain allowable matter as set forth below.

Claims 6, 13, 20 and 21 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant is advised the indication of allowable matters is made based on the scope as a whole, and that any change to the scope of these claims may jeopardize this indication of allowable subject matter.

The following is a statement of reasons for the indication of allowable subject matter:

15 As per claim 6, the trigger values correspond "to processor ID values in said system under test."

As per claim 13, "that for each of entry signals associated with each word from said each word only a predetermined one of said time stamp values is passed."

20 As per claims 20 and 21, "passing said selected down bytes in an entry word predetermined to contain data of interest into a byte stuffer as an abbreviated entry word, and stuffing said abbreviated entry words into a stuffed word entry for transfer into a high speed FIFO memory."

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P Bonzo whose telephone number is (703)305-4834. The examiner can normally be reached on Monday through Friday from 5:30AM
5 to 2:00PM.

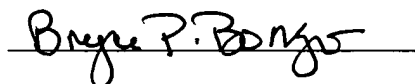
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel, can be reached on (703) 305-9713. For facsimile transmission:

After-final (703) 746-7238

Official (703) 746-7239

Non-Official/Draft (703) 746-7240

10 Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

A handwritten signature in black ink, reading "Bryce P. Bonzo", is written over a horizontal line.

Bryce Patrick Bonzo
Patent Examiner